IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO. 065686-0161

OIPE JUN 08 2006 PATENT & TRADEMARK OFFICE

Applicants: Tadashi MAEDA et al.

Title: PLL CIRCUIT

Appl. No.: 10/535,706

Filing Date: 05/20/2005

Examiner: Unassigned

Art Unit: 2817

Confirmation Number: 4199

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56.

A copy of each non-U.S. patent document and each non-patent document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), before the mailing date of the first Office Action on the merits, and within three (3) months of the mailing date of the foreign Office Action.

CONCISE EXPLANATION OF RELEVANCE

The documents listed on the attached PTO/SB/08 were cited as being relevant during the prosecution of the corresponding Japanese application. A partial English translation of the Japanese Office Action of May 10, 2006, follows:

- Claims 1, 2, 5
- Cited Literature 1, 2
- Remarks

When comparing the inventions of Claims 1, 2, and 5 of this application and the invention described in Literature 1 (Figures 2–5), they differ in that the invention described in Literature 1 is a PLL circuit comprising a single voltage controlled oscillator that has variable frequency ranges that overlap with one another, wherein the oscillation frequency is controlled by a phase difference signal, while the inventions described in Claims 1, 2, and 5 of this application are PLL circuits comprising multiple voltage controlled oscillators that have variable frequency ranges that overlap with one another, wherein the oscillation frequency is controlled by a phase difference signal.

Consequentially, examining the difference described above, Literature 2 describes a PLL circuit comprising multiple voltage controlled oscillators that have variable frequency ranges that overlap with one another, wherein the oscillation frequency is controlled by a phase difference signal (see Figures 2 and 6).

Here, because the invention described in Literature 1 and the invention described in Literature 2 share the common problem of providing a PLL with a wide capture range, the idea of configuring the single voltage controlled oscillator in the invention described in Literature 1 as the multiple voltage controlled oscillators described in Literature 2 is a matter that could have been easily conceived by a person having ordinary skill in the art.

- Claim 3
- Cited Literature 1, 2
- Remarks

Because no special technical significance is recognized in using multiple oscillators with mutually differing operating threshold voltage levels, an inventive step is not recognized in the invention of this claim.

Therefore, the invention of Claim 3 of this application could have been easily conceived by a person having ordinary skill in the art based on the inventions described in Literature 1 and 2.

- Claim 6
- Cited Literature 1–3
- Remarks

When comparing the invention of Claim 6 of this application and the inventions described in Literature 1 and 2, they differ in that the inventions described in Literature 1 and 2 do not have a means for setting two threshold voltages that differ from one another in the variable voltage range of the phase control voltage and for temporarily setting the level of this phase control voltage to a range bound by these two threshold voltages when the selection state of the voltage control oscillators changes.

Consequentially, examining the difference described above, the means for setting two threshold voltages that differ from one another in the variable voltage range of the phase control voltage and for temporarily setting the level of this phase control voltage to a range bound by these two threshold voltages when the selection state of the voltage control oscillators changes is publicly known technology, as described in Figure 3 of Literature 3, for example.

Therefore, the idea of establishing the configuration of the invention of Claim 6 of this application by applying the publicly known technology described in Literature 3 above to the invention described in Literature 1, to which the invention described in Literature 2 is applied, is a matter that could have been implemented at the discretion of a person having ordinary skill in the art.

- Claims 11, 13, 14
- Cited Literature 1, 3, 4
- Remarks

When comparing the inventions of Claims 11, 13, and 14 of this application and the invention described in Literature 1 (Figures 2–5), they differ in that the invention described in Literature 1 is a PLL circuit comprising a voltage controlled oscillator that has variable frequency ranges that overlap with one another, wherein the oscillation frequency is controlled by a phase difference signal, while the inventions described in Claims 11, 13, and 14 of this application are PLL circuits comprising a voltage controlled oscillator in which the oscillation frequency is controlled by multiple resonant circuits that have mutually differing resonant frequencies and a phase control signal.

Consequentially, examining the difference described above, a voltage controlled oscillator that comprises two resonant circuits that resonate at mutually differing resonant frequencies and is configured as a circuit that selects one of the resonant circuits is publicly known technology, as described in Figure 1 of Literature 4, for example.

Therefore, the idea of establishing the configuration of the invention of Claim 11 of this application by applying the publicly known technology described in Literature 4 above to the invention described in Literature 1 is a matter that could have been implemented at the discretion of a person having ordinary skill in the art.

Other points are as stated in the sections for Claims 1, 2, 5, and 6 above.

- Claims 19, 21, 22
- Cited Literature 1, 3, 5
- Remarks

When comparing the inventions of Claims 19, 21, and 22 of this application and the invention described in Literature 1 (Figures 2–5), they differ in that the invention described in Literature 1 is a PLL circuit comprising a voltage controlled oscillator that has variable frequency ranges that overlap with one another, wherein the oscillation frequency is controlled by a phase difference signal, while the inventions described in Claims 19, 21, and 22 are PLL circuits comprising a voltage controlled oscillator that is configured with multiple connected delay circuits in which the delay times are controlled by phase control signals.

Consequentially, examining the difference described above, a voltage controlled oscillator that is configured with multiple connected delay circuits in which the delay times are controlled by phase control signals is publicly known technology, as described in Figure 1 of Literature 5, for example.

Therefore, the idea of establishing the configuration of the invention of Claim 19 of this application by applying the publicly known technology described in Literature 5

above to the invention described in Literature 1 is a matter that could have been implemented at the discretion of a person having ordinary skill in the art.

Other points are as stated in the sections for Claims 1, 2, 5, and 6 above.

- Claims 27
- Cited Literature 1
- Remarks

The invention of Claim 27 of this application does not effectively differ from the invention described in Literature 1, and it could have been easily conceived by a person having ordinary skill in the art based on the invention described in Literature 1.

List of Cited Literature

1. Japanese Unexamined Patent Application Publication 2001-60870
2. Japanese Unexamined Patent Application Publication H06-303134
3. Japanese Unexamined Patent Application Publication H09-246962
4. Japanese Unexamined Patent Application Publication 2001-237640
5. Japanese Unexamined Patent Application Publication 2001-94417

Record of Prior Art Literature Search Results

- Fields Searched

IPC H03L 7/06–7/23

- Prior Art Literature

Japanese Unexamined Patent Application Publication 2001-144609
Japanese Unexamined Patent Application Publication 2001-2337699
Microfilm of Japanese Utility Model Application H2-11776 (Japanese Unexamined Utility Model Application Publication H3-103611)
Microfilm of Japanese Utility Model Application S58-51935 (Japanese Unexamined Utility Model Application Publication S59-157317)
Japanese Unexamined Patent Application Publication H1-123508

(The Record of Prior Art Literature Search Results does not constitute a reason for rejection.)

STATEMENT

The undersigned hereby states in accordance with 37 CFR §1.97(e)(1) that each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to filing of this Statement.

The undersigned hereby states in accordance with 37 CFR §1.704(d) that each item of information contained in the information disclosure statement was first cited in a communication from a foreign patent office in a counterpart application and that this

communication was not received by any individual designated in 37 CFR §1.56(c) more than thirty days prior to the filing of the information disclosure statement.

Although Applicants believe that no fee is required for this Request, the Commissioner is hereby authorized to charge any additional fees which may be required for this Request to Deposit Account No. 19-0741.

Respectfully submitted,

June 8, 2006
Date

David A. Blumenthal
Attorney for Applicant
Registration No. 26,257

Reg. No. 43,438

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 672-5407
Facsimile: (202) 672-5399

MODIFIED PTO/SB/08 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	10/535,706
Date Submitted: June 8, 2006				**Filing Date**	11/21/2003
				First Named Inventor	Tadashi MAEDA, et al.
(use as many sheets as necessary)				**Group Art Unit**	2817
				Examiner Name	Unassigned
Sheet	1	of	1	**Attorney Docket Number**	065686-0161

OIPE IAP13 JUN 08 2006 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (*if known*)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	B1	6,411,168		YOSHIDA	06-25-2002	
	B2	6,687,321		KADA et al.	02-03-2004	
	B3	6,714,772		KASAHARA et al.	03-30-2004	

UNPUBLISHED U.S. PATENT APPLICATION DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Application Document Serial Number	U.S. Patent Application Document Kind Code[2] (*if known*)	Name of Patentee or Applicant of Cited Document	Filing Date of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (*if known*)	Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	B4	JP	59-157317			10-22-1984		
	B5	JP	01-123508		MITSUBISHI ELECTRIC CORP	05-16-1989		Abst.
	B6	JP	03-103611			10-28-1991		
	B7	JP	06-303134		HITACHI LTD.	10-28-1994		Abst.
	B8	JP	09-246962		NEC CORPORATION	09-19-1997		Abst.
	B9	JP	2001-060870		MATSUSHITA ELECTRIC IND. CO. LTD.	03-06-2001		Abst.
	B10	JP	2001-094417		TOSHIBA MICROELECTRONICS CORP.	04-06-2001		Abst.
	B11	JP	2001-144609		SANYO ELECTRIC CO. LTD.	05-25-2001		Abst.
	B12	JP	2001-237640		MURATA MFG CO, LTD.	08-18-2001		Abst.
	B13	JP	2001-237699		HITACHI LTD.	08-31-2001		Abst.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.